Drive for better vision


# 奇景盃

# IC Layout 競賽

# Design Rule

**Version 4.0**

# Modify History

| Ver. | Eff_Date | Author | Change Description |
|---|---|---|---|
| 1.0 | 2005/1/21 | C.L Wu | New create |
| 1.2 | 2006/1/23 | C.L Wu | Add P+OD Device can't inside Psub |
| 1.3 | 2008/1/20 | C.L Wu | Change the front cover |
| 2.0 | 2008/6/5 | C.L Wu | Change rules base , new create design rules |
| 3.0 | 2010/12/1 | C.L Wu | Add DNW layer rules |
| 3.1 | 2012/2/6 | C.L Wu | Modify VIA2.E.1 &VIA2.E.2 |
| 4.0 | 2013/12/15 | C.L Wu | 1.Add Device & Well Junction Breakdown Voltage<br>2.Modify OD.S.2, PP.E.1, PP.C.5, NP.E.1, NP.C.5,OD.C.2,OD.C.4 |

# INTRODUCTION

## 1.1 Reserved Layer Names

| GDSII name | purpose | layer no. | Layer usage description |
|---|---|---|---|
| **NWELL** | **drawing** | **3;0** | **Nwell** |
| **DNW** | **drawing** | **4:0** | **Define LV/MV Device tri-well** |
| **OD** | **drawing** | **6;0** | **Definition of diffusion areas such as source, drain and interconnect** |
| **PIMP** | **drawing** | **25;0** | **P+ implantation definition** |
| **NIMP** | **drawing** | **26;0** | **N+ implantation definition** |
| **POLY1** | **drawing** | **17;0** | **Definition of MOS poly gate** |
| **POLY2** | **drawing** | **14;0** | **POLY2, Capacitor top poly-Si** |
| **OD2** | **drawing** | **15:0** | **Thick oxide for a device** |
| **RPO** | **drawing** | **29:0** | **Silicide protection** |
| **CONT** | **drawing** | **30;0** | **Definition of contact window from M1 to OD or PO** |
| **MT1** | **drawing** | **31;0** | **Metal1** |
| **VIA1** | **drawing** | **51;0** | **Definition of VIA hole from M2 to M1** |
| **MT2** | **drawing** | **32;0** | **Metal2** |
| **VIA2** | **drawing** | **52;0** | **Definition of VIA hole from M3 to M2** |
| **MT3** | **drawing** | **33;0** | **Metal3** |
| VIA3 | **drawing** | **53:0** | **Definition of VIA hole from M4 to M3** |
| MT4 | **drawing** | **34:0** | **Metal4 (Top Metal)** |
| CB | **drawing** | **43;0** | **Passivation Window** |
| **BJTDMY** | **drawing** | **110;0** | **BJT dummy layer for LVS.** |
| **DIODMY** | **drawing** | **119;0** | **DIODE dummy layer for LVS.** |
| **RDMY** | **drawing** | **115;0** | **RES dummy layer for LVS.** |

| | | | |
|---|---|---|---|
| **MT1** | **drawing** | **31;0** | **For LVS Check text layer 31 attach MT1** |
| **MT2** | **drawing** | **32;0** | **For LVS Check text layer 32 attach MT2** |
| **MT3** | **drawing** | **33;0** | **For LVS Check text layer 33 attach MT3** |
| **MT3** | **drawing** | **34;0** | **For LVS Check text layer 34 attach MT4** |

## 1.2 Terminology Defintions

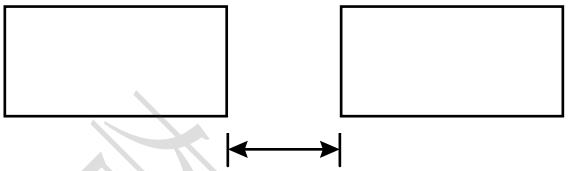
The following definitions are used in the physical design rules :

N+ OD : OD covered with NIMP.
P+ OD : OD covered with PIMP.
Cold N-Well : N-Well connected to the most positive voltage (VDD).
Hot N-Well : N-Well not connected to the most positive voltage
Hot N+ diffusion : all N+ diffusion regions outside the N-Well which have a potential not equal to the substrate voltage.
Hot P+ diffusion : all P+ diffusion regions inside the N-Well which have a potential not equal to the N-Well potential.
Outside N-Well : a diffusion which has the potential the same as the substrate.
Inside N-Well : a diffusion which has the potential the same as the N-Well.

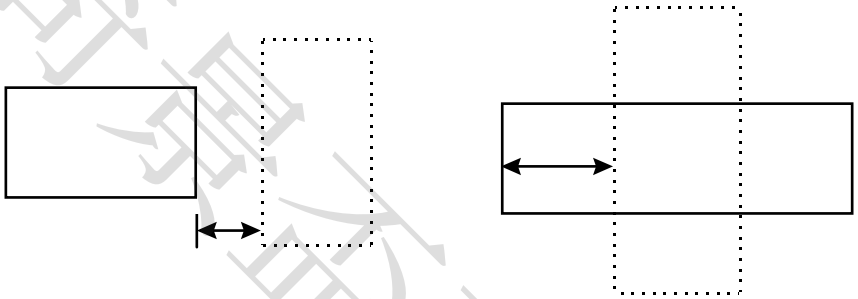
## 1.3 Definition of the layout layers

WIDTH :

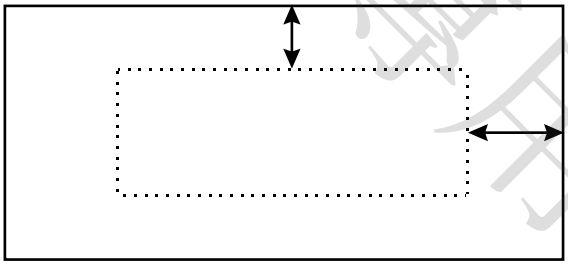
SPACE :



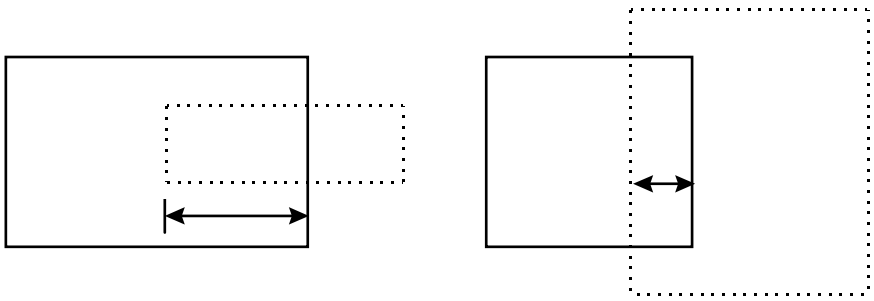
CLEARANCE :



EXTENSION :



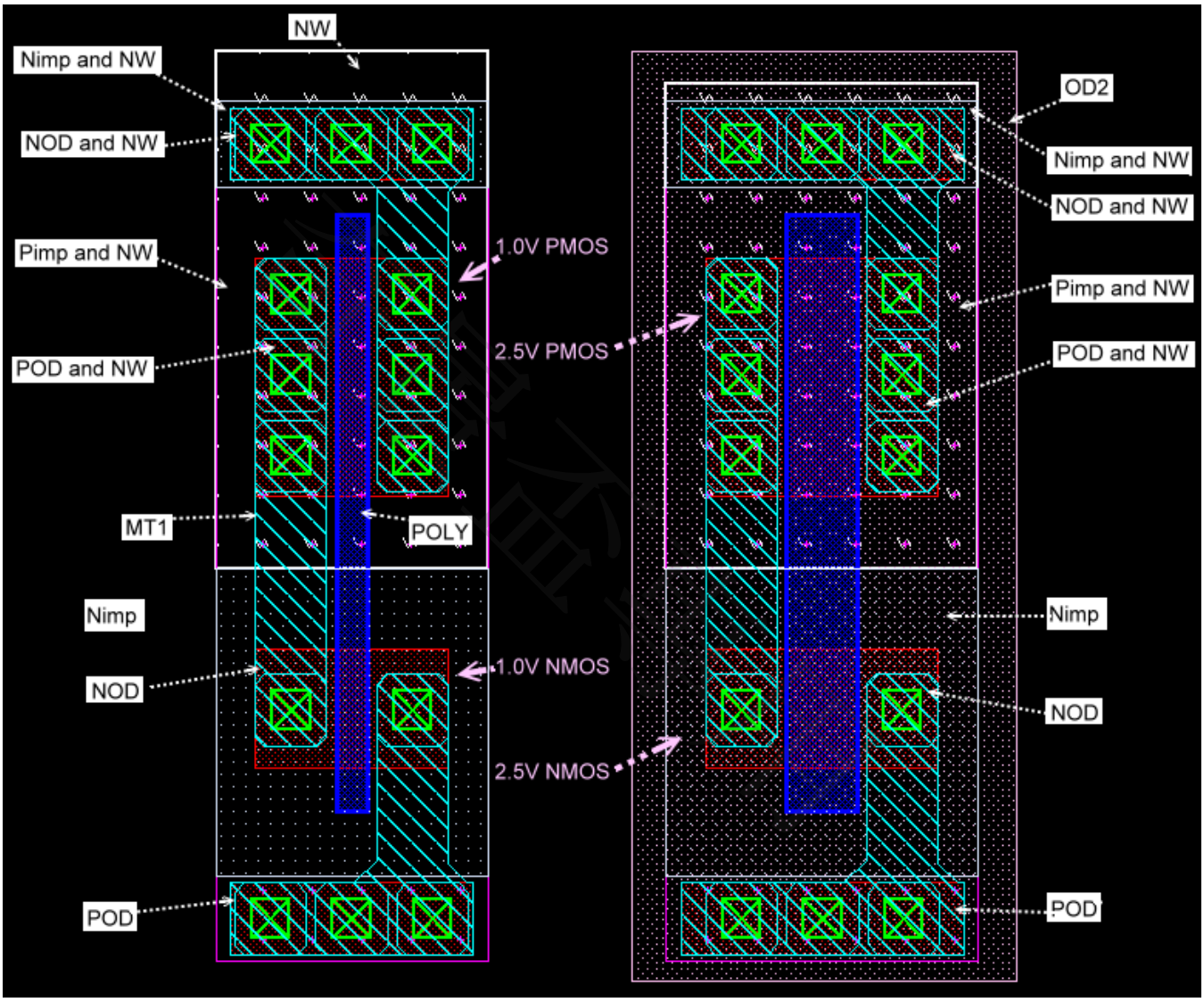
OVERLAP :



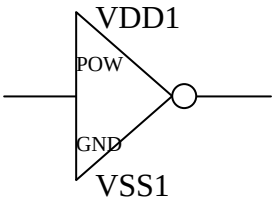
## 2. Device Layout Format

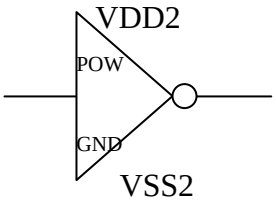
*P type Device(MOS/RES/DIO….) 請勿直接放於 P-sub/Pwell 上 (需放於 NWELL 內)

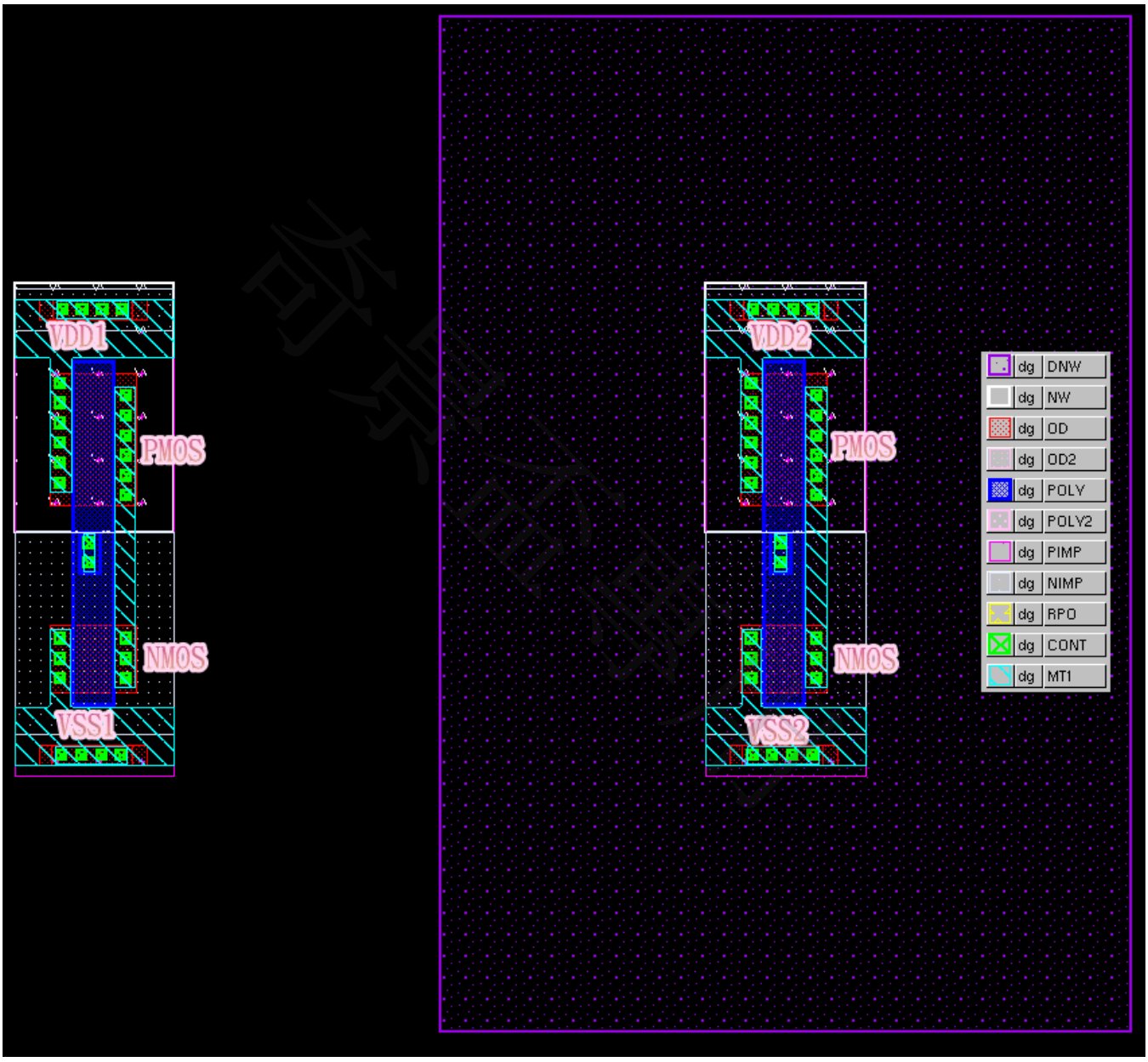
### MOS:



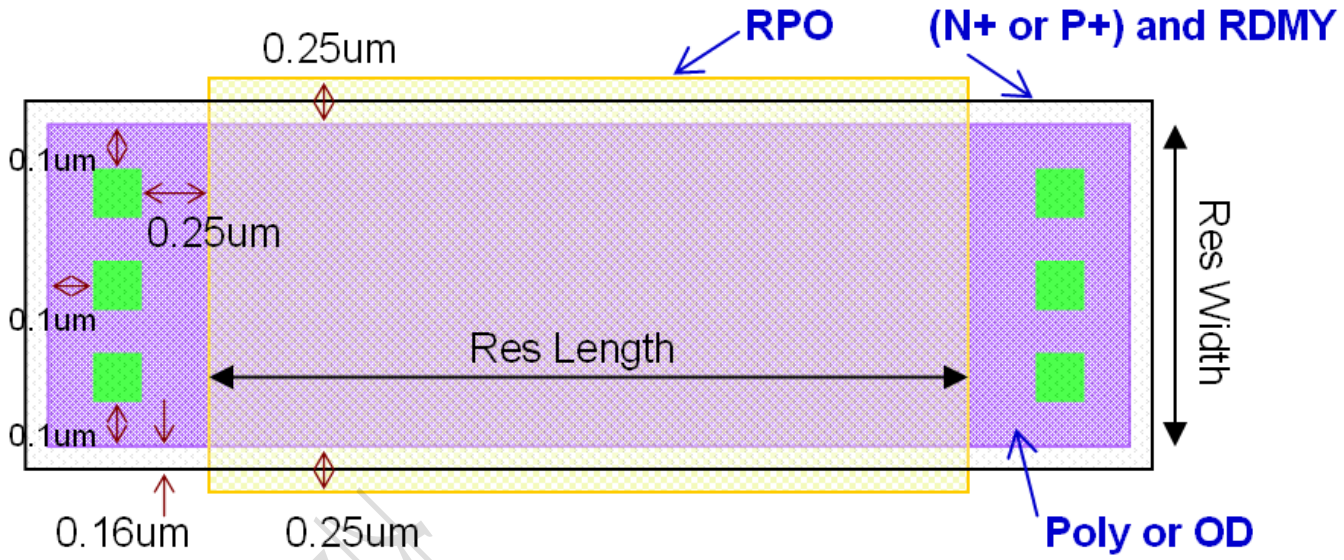
## Multi-P/G Layout sample



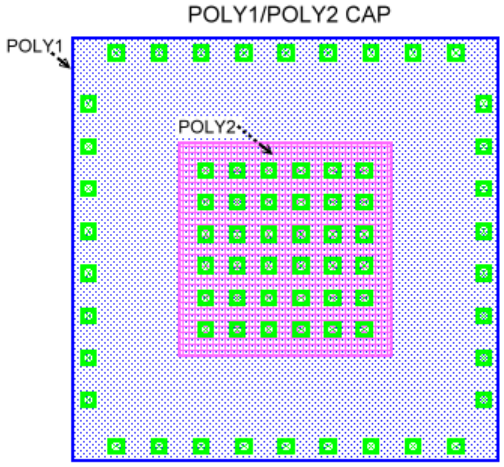



## RESISTOR:



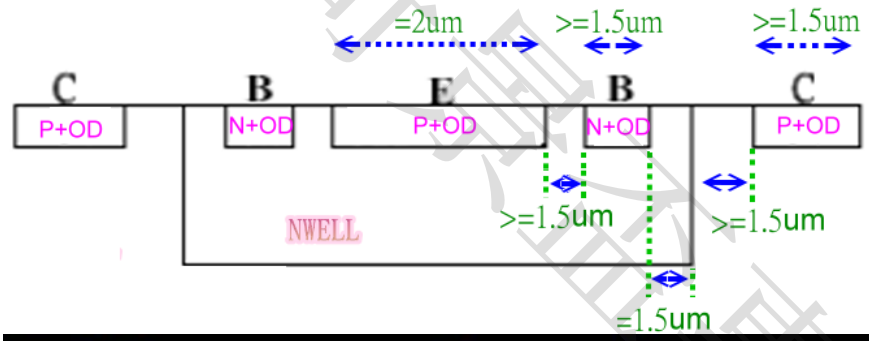

| Type name | Layer | Ohms/sq |
|---|---|---|
| PPOR | Poly and RPO and Pimp | 300 |
| NPOR | Poly and RPO and Nimp | 320 |
| PODR | OD and RPO and Pimp | 125 |
| NODR | OD and RPO and Nimp | 145 |

## CAPACITOR:




Cap = Ca*Polycap_area+Cf*Polycap_peri
Polycap_area = Area of POLY1 Overlap POLY2
Polycap_peri = Periphery of POLY1 Overlap POLY2
Ca = 50E-5 pF/umsq
Cf = 10E-5 pF/um

## Bipolar junction transistor

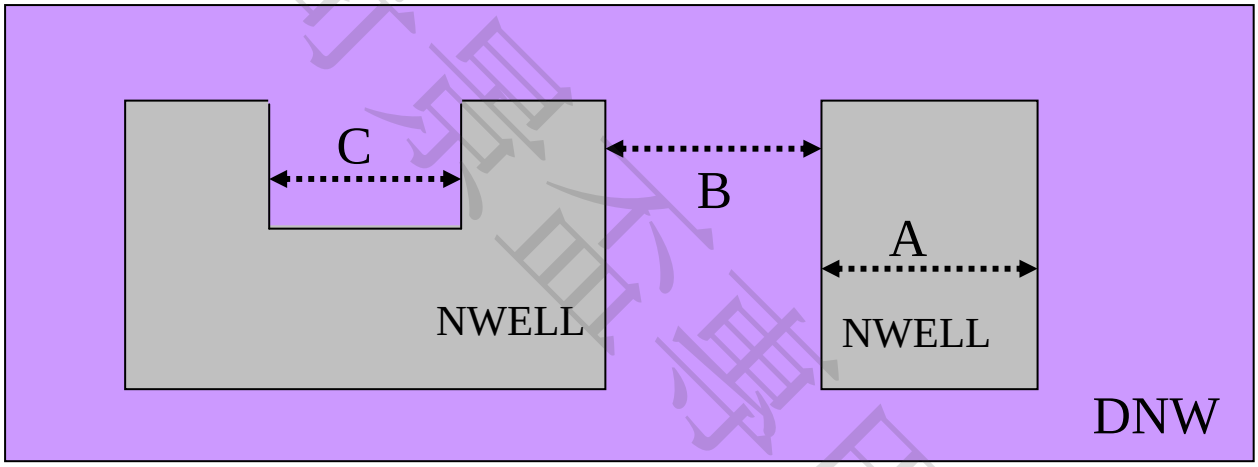


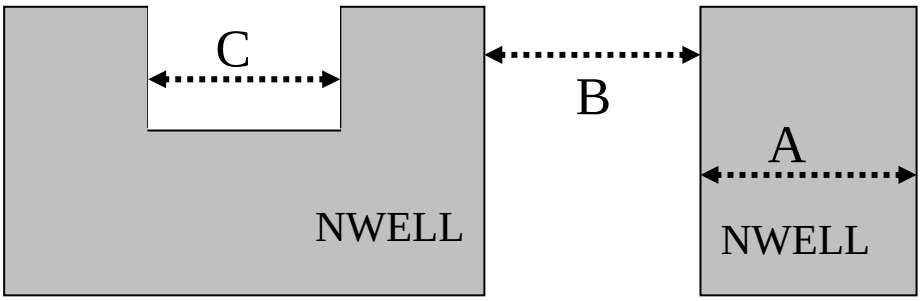

# 3. Layout Rule Description

## NWELL Rule

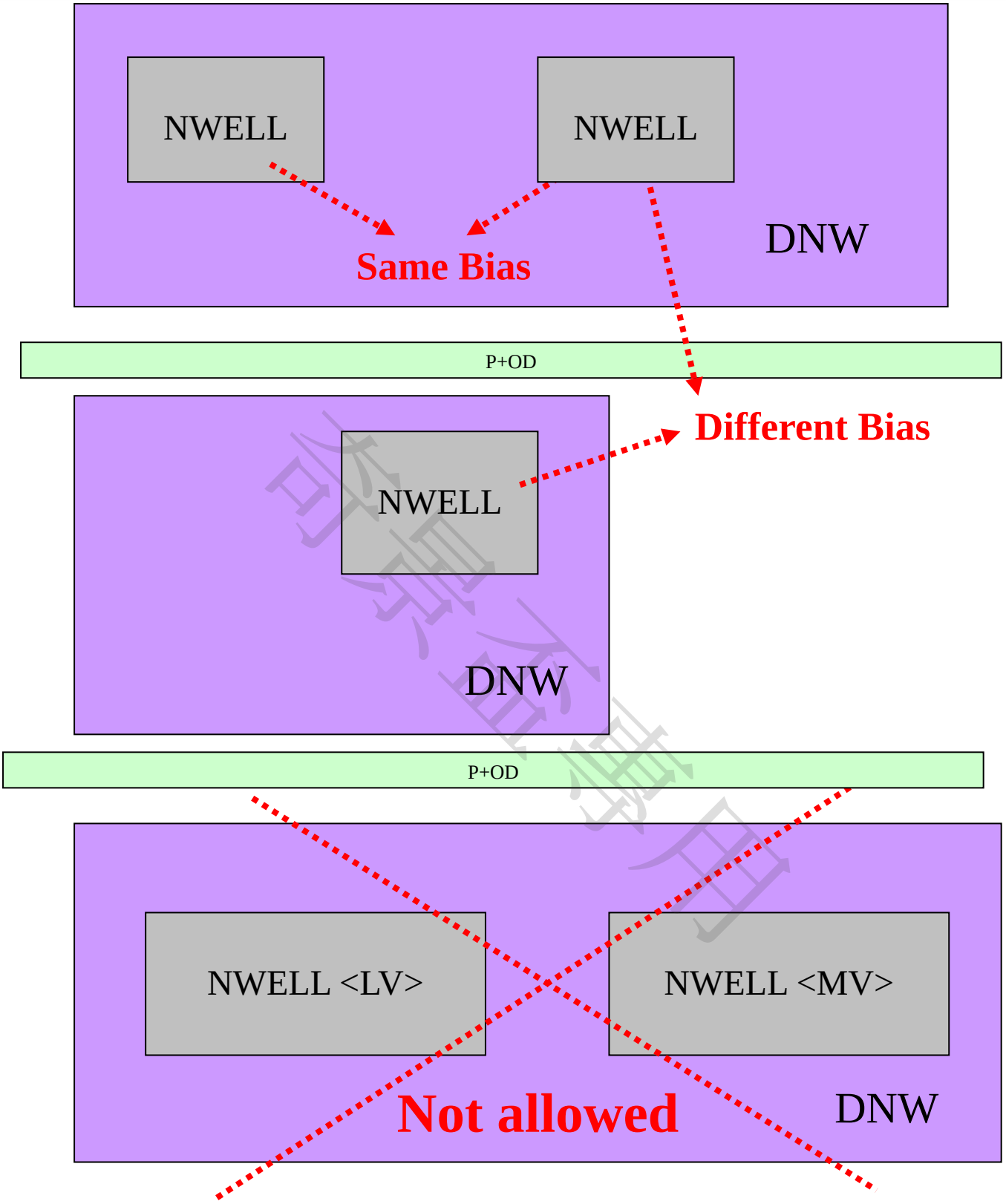
| Rule No. | Description Layout | Rule |
|---|---|---|
| Layer : NWELL | N-Well | |
| NW.W.1 | Minimum dimension of a NW region | A >= 0.7um |
| NW.S.1 | Minimum space between two NW regions | B >= 1.2 um |
| NW.N.1 | Minimum notch | C >= 0.8um |

**Recommend not using unintentional floating well.**




PSUB

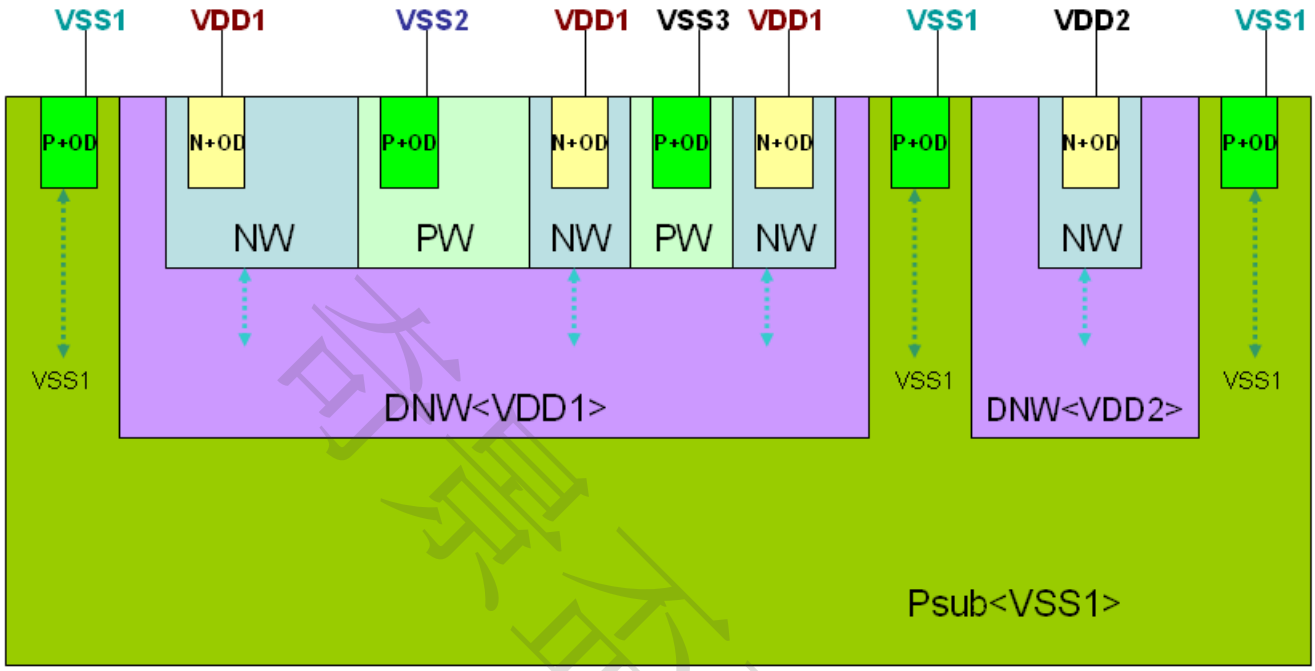


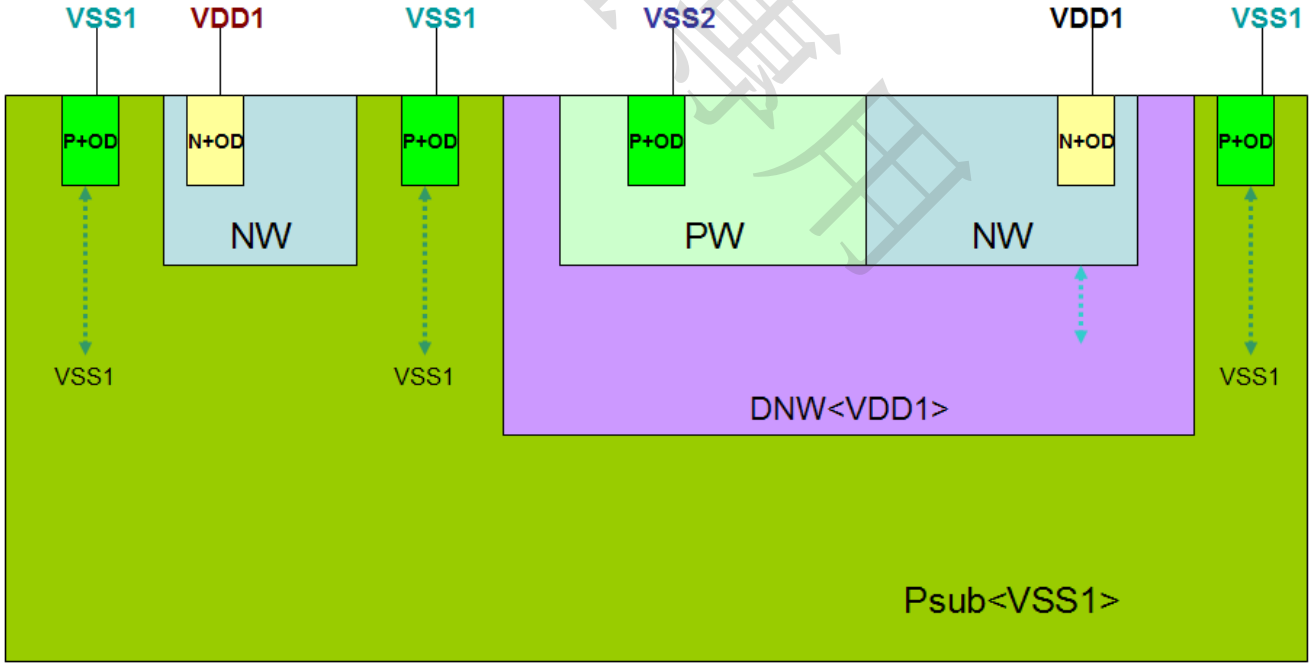

Note：

1. NWELL with different potential must be separated by a different DNW
2. The potential of different NWELLs inside the same DNW are identical

# Cross view

**For example : Power => VDD1、VDD2 , Gnd ➔ VSS1、VSS2、VSS3**
**VSS1 = Psub**

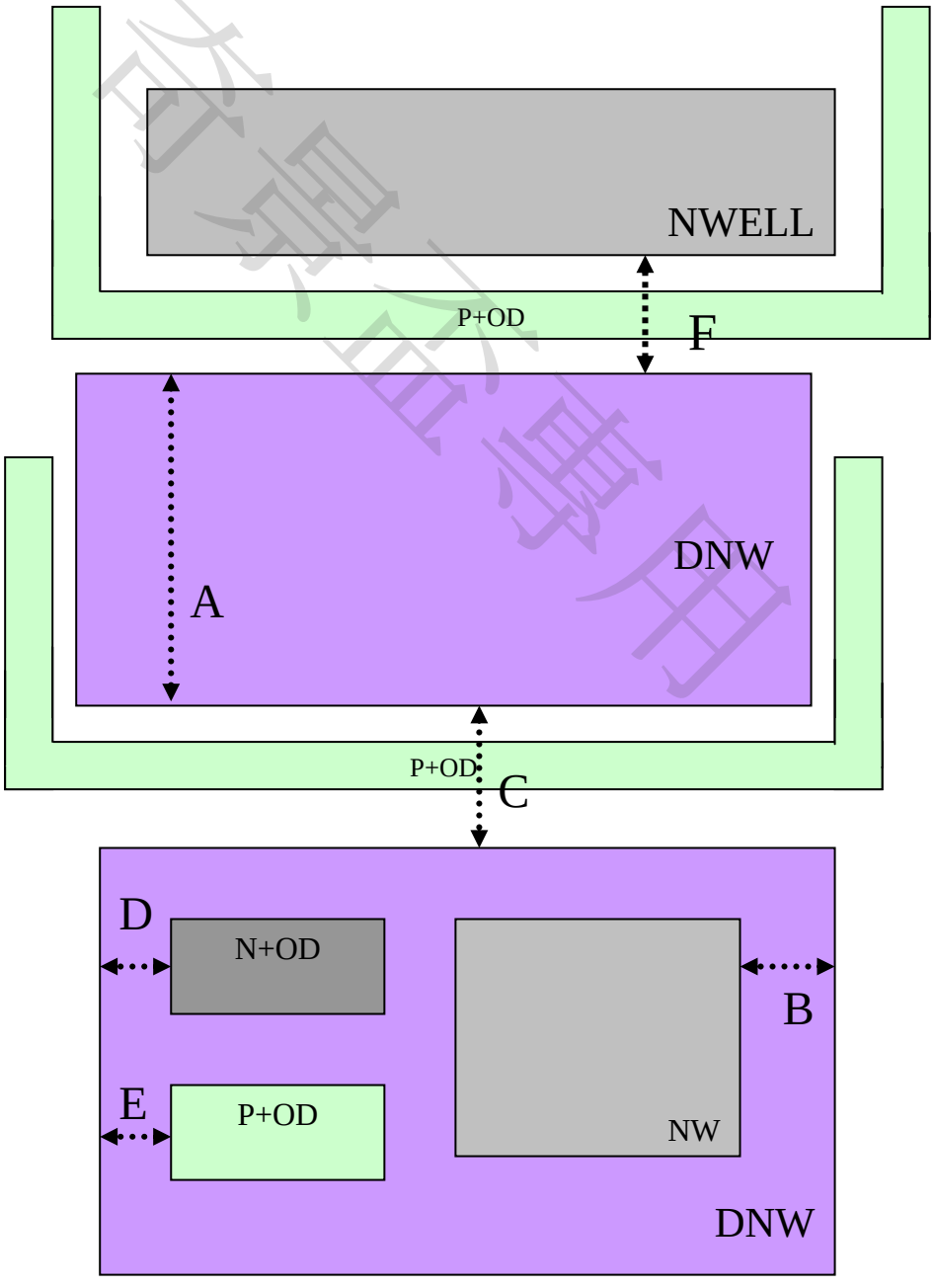



**Note：PW is operated by mask tooling，not drawing layer，**
**as follows ： PW= (size DNW by -1.5) not NW**

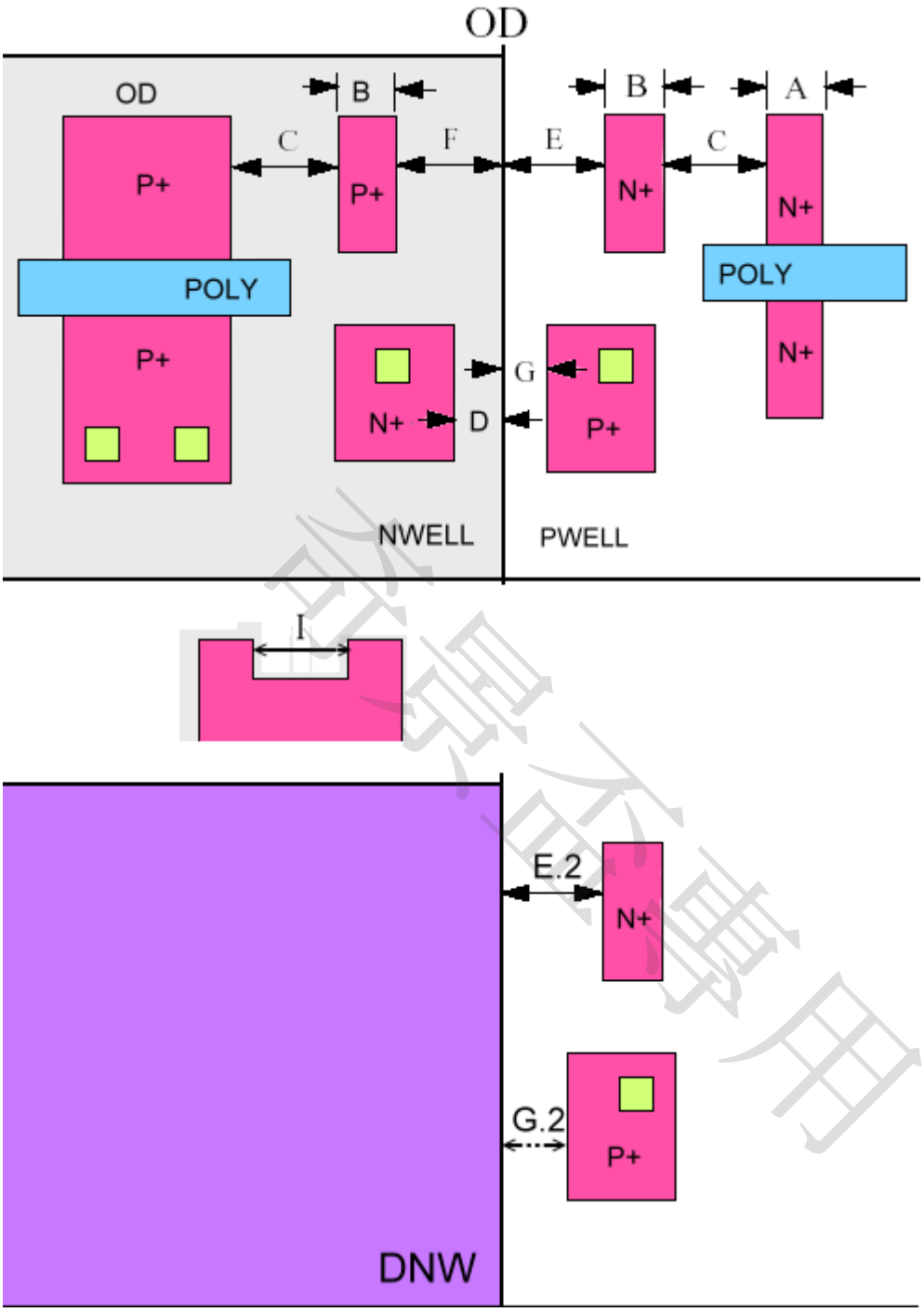
## DNW Rule

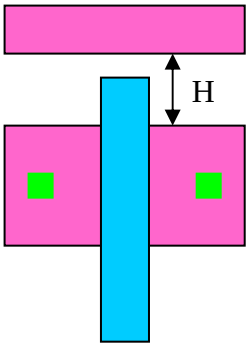
| Rule No. | Description Layout | Rule |
|---|---|---|
| Layer : DNW | Deep NWELL | |
| DNW.W.1 | Minimum width of DNW region | A >= 3um |
| DNW.E.1 | Minimum extension from DNW to NWELL | B >= 2 um |
| DNW.S.1 | Minimum space between two DNW regions | C >= 4.5um |
| DNW.E.2 | Minimum extension from DNW region to N+OD region which is outside NWELL region | D >= 3.5 um |
| DNW.E.3 | Minimum extension from DNW region to P+OD region which is outside NWELL region | E >= 3.2um |
| DNW.S.2 | Minimum space of NWELL to DNW | F >= 4um |



## Thin Oxide Rule

| Rule No. | Description Layout | Rule |
|---|---|---|
| Layer : OD | Thin Oxide Definition | |
| OD.W.1 | Minimum width of an OD region to define the width of NMOS/PMOS | A >= 0.14 um |
| OD.W.2 | Minimum width of an OD region for interconnect (N+/or P+) | B >= 0.14 um |
| OD.S.1 | Minimum space between two OD regions | C >= 0.21 um |
| OD.C.1 | Minimum clearance from NWELL edge to a N+ OD region which is inside the NWELL | D >= 0.25 um |
| OD.C.2 | Minimum clearance from NWELL edge to a N+ OD region which is outside NWELL | E >= 0.5 um |
| OD.C.3 | Minimum clearance from DNW edge to a N+ OD region which is outside DNW | E.2 >= 1.5 um |
| OD.C.4 | Minimum clearance from NWELL edge to a P+ OD region which is inside a NWELL | F >= 0.5 um |
| OD.C.5 | Minimum clearance from NWELL edge to a P+OD region (for PW pick up) which is outside a NWELL | G >= 0.3 um |
| OD.C.6 | Minimum clearance from DNW edge to a P+OD region which is outside a DNW | G.2 >=1 um |
| OD.S.2 | Minimum space of LV MOS to Guard Ring<br>Minimum space of MV MOS to Guard Ring | H >= 0.36 um<br>H >= 0.46 um |
| OD.N.1 | Minimum notch | I >= 0.16 um |



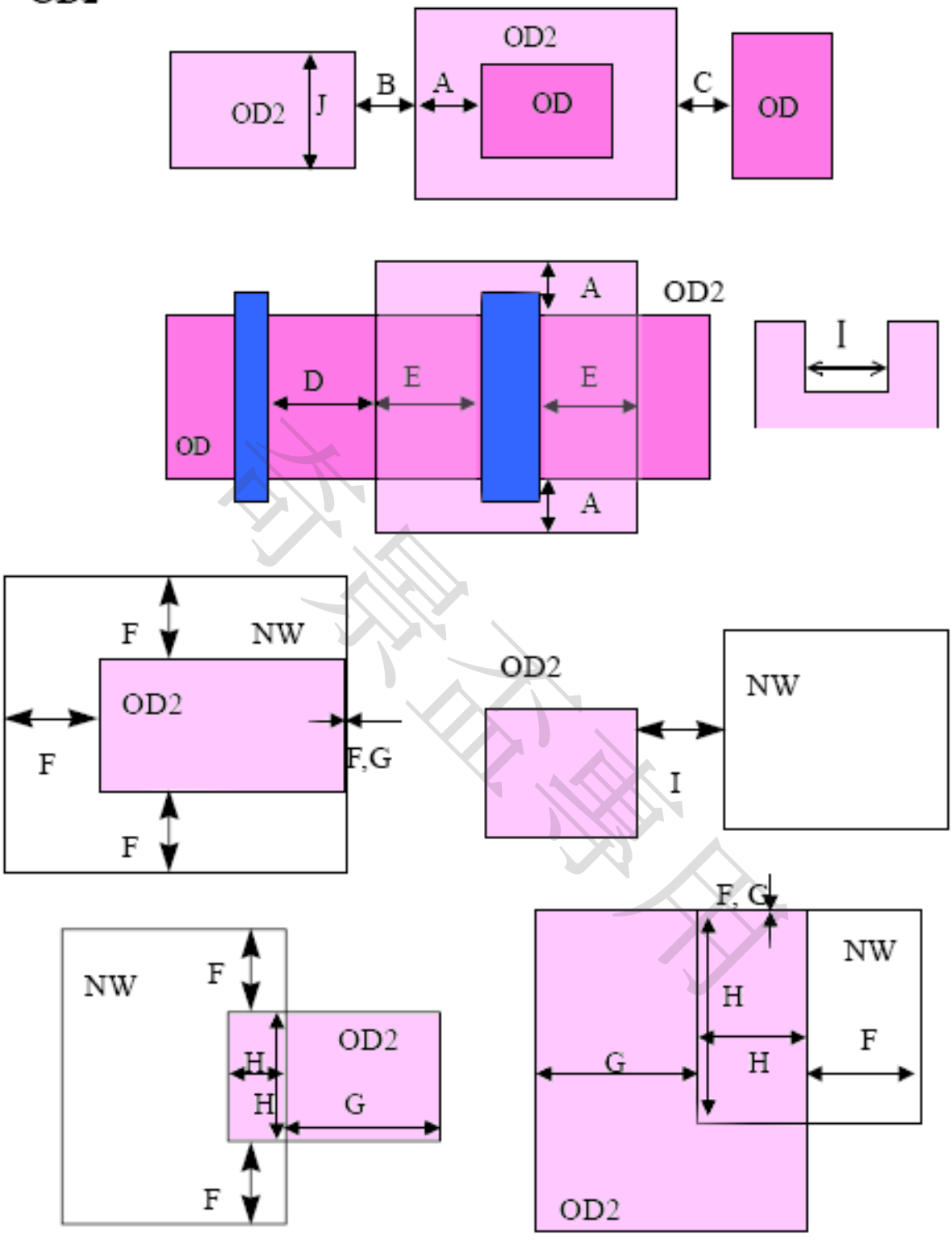



## Thick Oxide Rule

Definition 2.5V(MV) Device

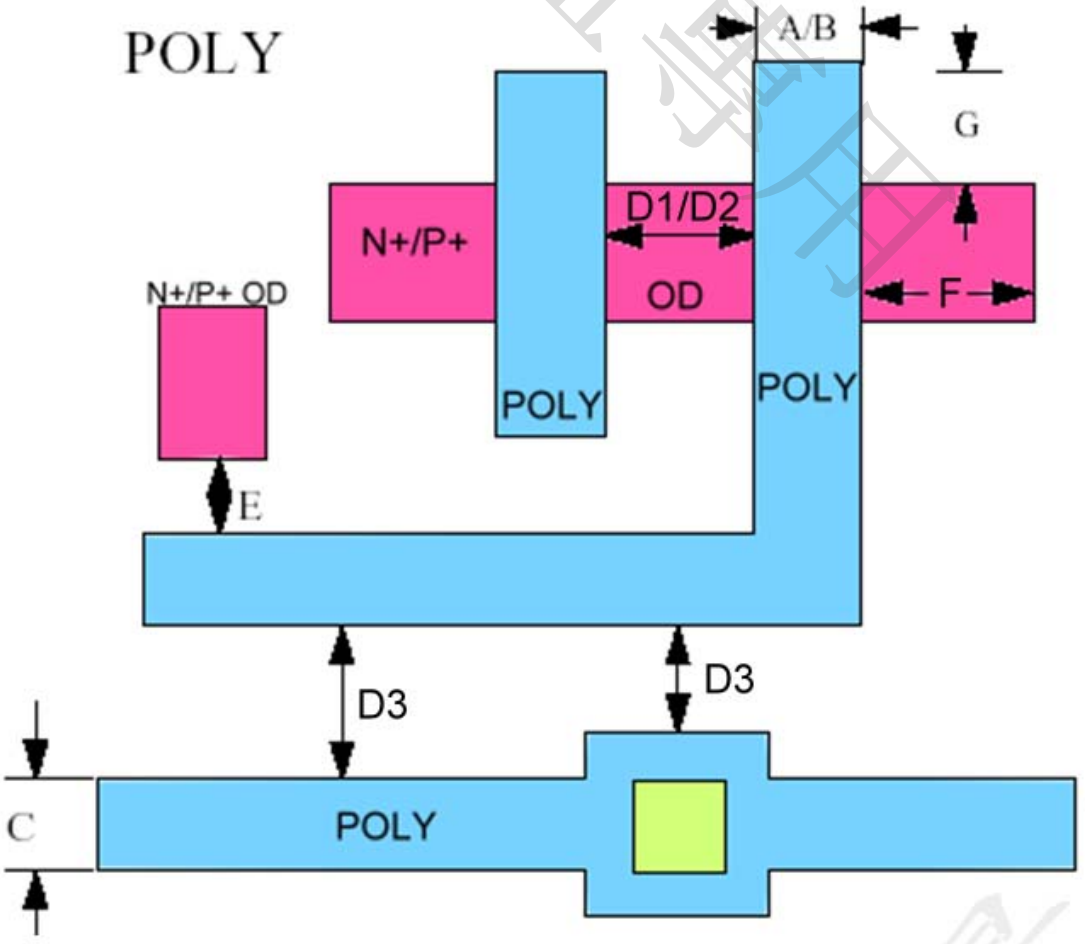
| Rule No. | Description Layout | Rule |
|---|---|---|
| Layer : OD2 | Thick Oxide Definition | |
| OD2.W.1 | Minimum width | J >= 0.65 um |
| OD2.S.1 | Minimum space | B >= 0.9 um |
| OD2.S.2 | Space to OD | C >= 0.3 um |
| OD2.S.3 | Space to 1.0V device | D >= 0.3 um |
| OD2.S.4 | Space to NW , Space=0 is allowed | I >= 0.6 um |
| OD2.EN.1 | Enclosure of 2.5V Gate in S/D direction | E >= 0.3 um |
| OD2.EX.1 | Extension on device | A >= 0.3 um |
| OD2.EX.2 | NW extension on OD2 , extension=0 is allowed | F >= 0.6 um |
| OD2.EX.3 | Extension on NW , extension=0 is allowed | G >= 0.6 um |
| OD2.O.1 | Overlap of NW , Overlap = 0 is allowed | H >= 0.6 um |
| OD2.N.1 | Minimum notch | I >= 0.6 um |

## OD2



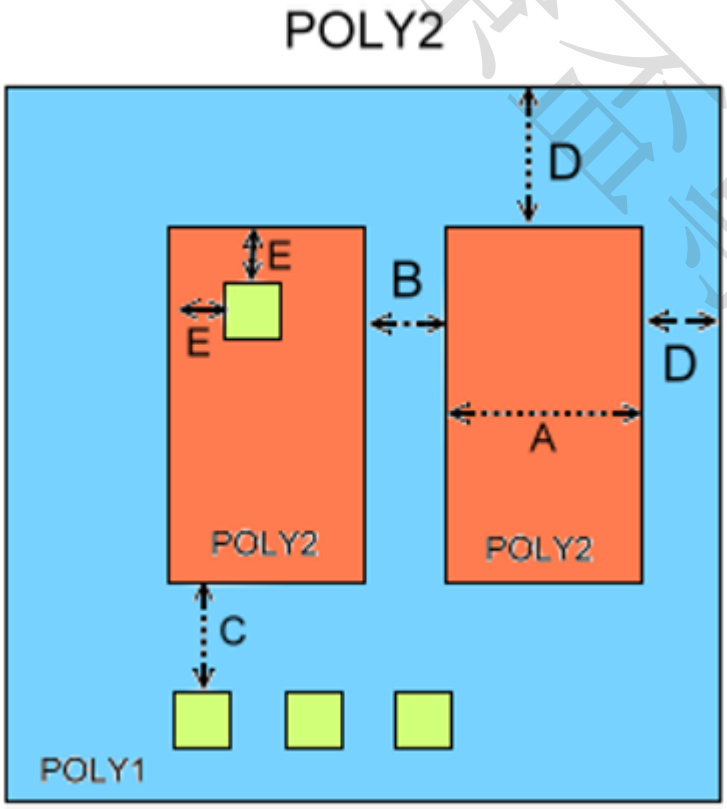
## Poly Rule

| Rule No. | Description Layout | Rule |
|---|---|---|
| Layer : POLY1 | Poly Si | |
| PO.W.1 | Minimum Channel length of 1.0V PMOS<br>Minimum Channel length of 2.5V PMOS | A. 0.13um<br>B. 0.2um |
| PO.W.2 | Minimum Channel length of 1.0V NMOS<br>Minimum Channel length of 2.5V NMOS | A. 0.13um<br>B. 0.2um |
| PO.W.3 | Minimum width of a PO region for interconnect. | C. 0.13 um |
| PO.S.1 | Minimum Gate space on 1.0V OD area.<br>Minimum Gate space on 2.5V OD area. | D1. 0.16 um<br>D2. 0.22 um |
| PO.S.2 | Minimum space between two PO regions on field oxide area. | D3. 0.17 um |
| PO.C.1 | Minimum clearance from an OD region to a PO on field oxide. | E. 0.08 um |
| PO.C.2 | Minimum clearance from a PO gate to a related OD edge | F. 0.22 um |
| PO.O.1 | Minimum overlap of a PO region extended into field oxide (endcap) | G. 0.18 um |



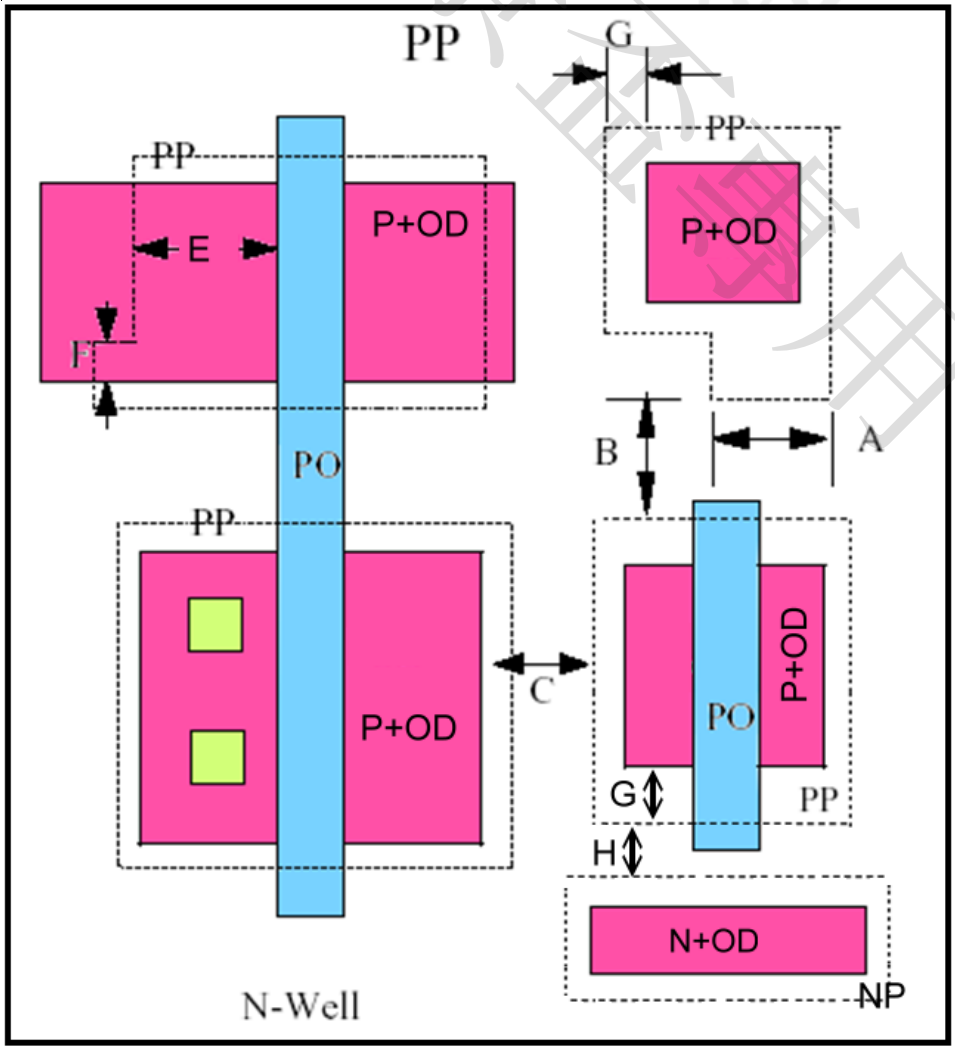
## Poly-2 Rule

| Rule. No. | Description Layout | Rule |
|---|---|---|
| Layer : PO2 | Poly-2 Si | |
| PO2.W.1 | Minimum width of a PO2 region for the capacitor top plate | A. 0.8 um |
| PO2.S.1 | Minimum space between two PO2 regions of capacitors | B. 0.6 um |
| PO2.C.1 | Minimum clearance from a CO on PO region as a capacitor bottom plate to a PO2 region as a capacitor top plate | C. 0.5 um |
| PO2.E.1 | Minimum extension of PO over PO2 as capacitor top plate | D. 1 um |
| PO2.E.2 | Minimum extension of a PO2 region as a capacitor top plate beyond a CO region | E. 0.3um |
| PO2.R.1 | PO2 on OD area is not allowed | |



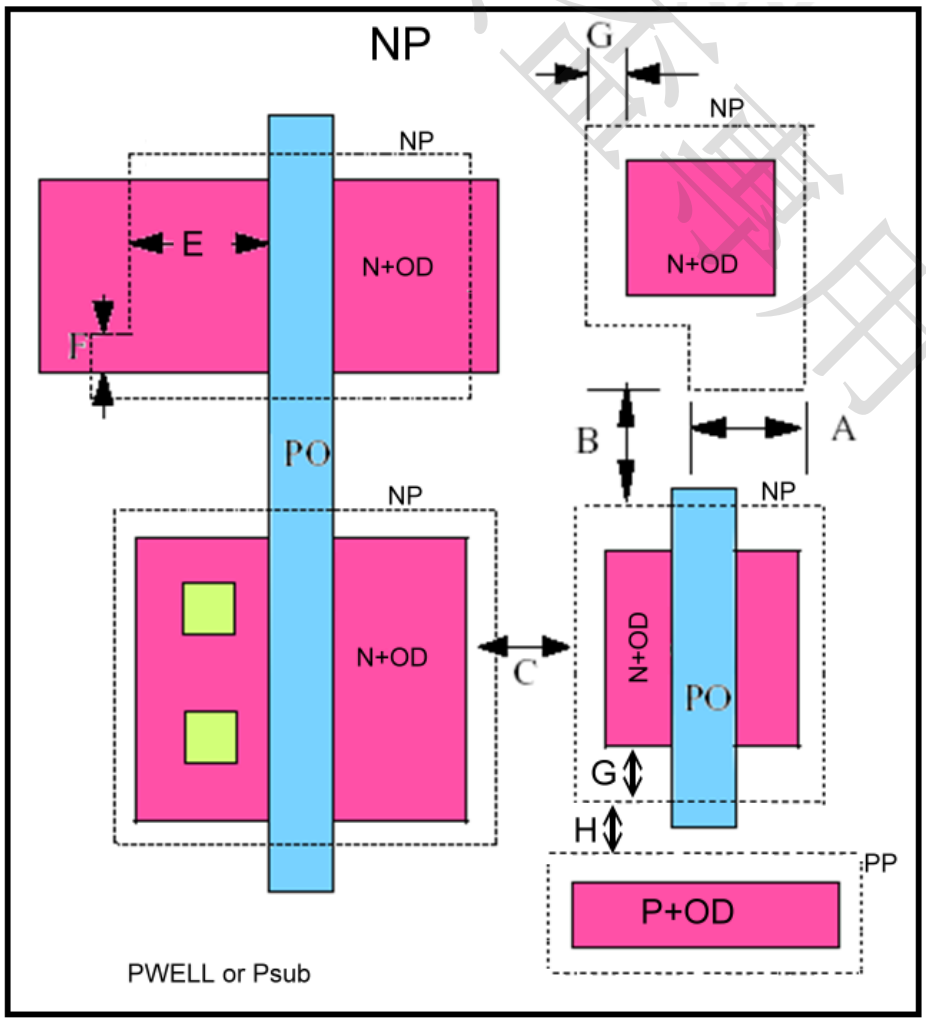
## P+ S/D Rule

| Rule No. | Description Layout | Rule |
|---|---|---|
| Layer : PIMP(PP) | P+ S/D Implantation | |
| PP.W.1 | Minimum width of a PP region | A >= 0.32 um |
| PP.S.1 | Minimum space between two PP regions Merge if the space is less than | B >= 0.32 um |
| PP.C.1 | Minimum clearance from a PP region to an OD region | C >= 0.16 um |
| PP.C.3 | Minimum clearance from a PP edge to a Pchannel PO gate | E >=0.42 um |
| PP.O.1 | Minimum overlap from a PP edge to an OD region | F >=0.2 um |
| PP.E.1 | Minimum extension of a PP region beyond a PP OD region. | G >=0.13 um |
| PP.C.5 | PP edge to NP edge space | H >=0.1 um |



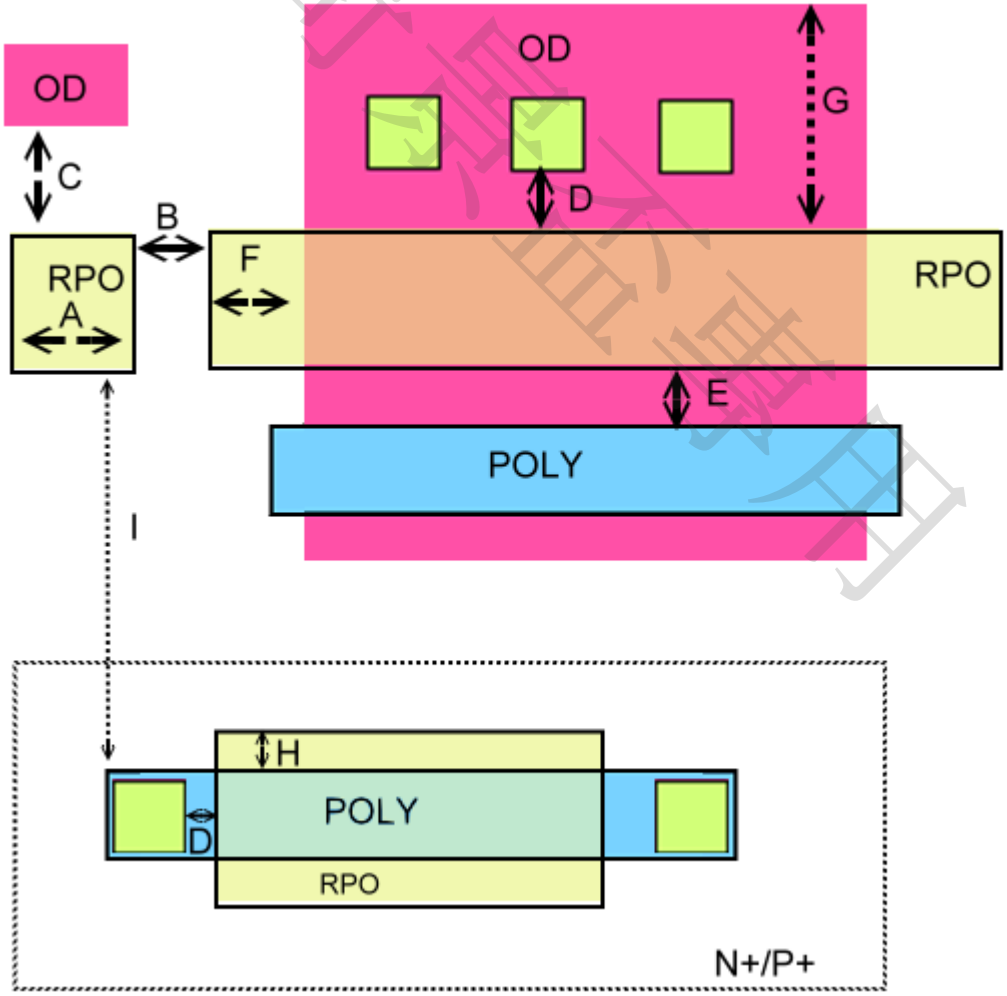
## N+ S/D Rule

| Rule No. | Description Layout | Rule |
|---|---|---|
| Layer : NIMP(NP) | N+ S/D Implantation | |
| NP.W.1 | Minimum width of a NP region | A >= 0.32 um |
| NP.S.1 | Minimum space between two NP regions Merge if the space is less than 0.6 um | B >= 0.32 um |
| NP.C.1 | Minimum clearance from a NP region to an OD region | C >= 0.16 um |
| NP.C.2 | Minimum clearance from a NP edge to a Nchannel PO gate | E >=0.42 um |
| NP.O.1 | Minimum overlap from a NP edge to an OD region | F >=0.2 um |
| NP.E.1 | Minimum extension of a NP region beyond a NP OD region. | G >=0.13 um |
| NP.C.5 | NP edge to PP edge space | H >=0.1 um |



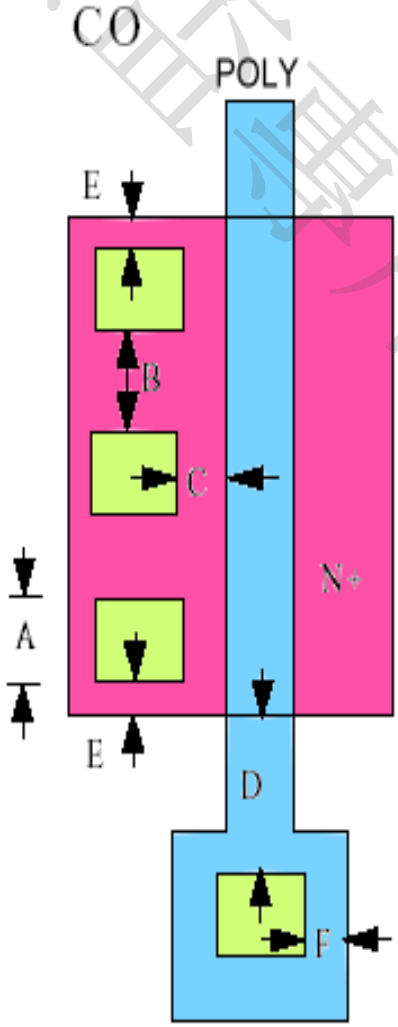
## RPO Rule

| Rule No. | Description Layout | Rule |
|---|---|---|
| Layer : RPO | Resist Protection Oxide | |
| RPO.W.1 | RPO width | A >= 0.45 um |
| RPO.S.1 | Space | B >= 0.45 um |
| RPO.S.2 | RPO to OD space | C >= 0.25 um |
| RPO.S.3 | RPO to CONT space | D >= 0.25 um |
| RPO.S.4 | RPO to Gate space | E >= 0.35 um |
| RPO.S.5 | Extension on unsilicided OD | F >= 0.25 um |
| RPO.EX.1 | OD extension on RPO | G >= 0.25 um |
| RPO.EX.2 | Poly extension on RPO | H >= 0.25 um |
| RPO.EX.3 | RPO to Poly space | I >= 0.3 um |



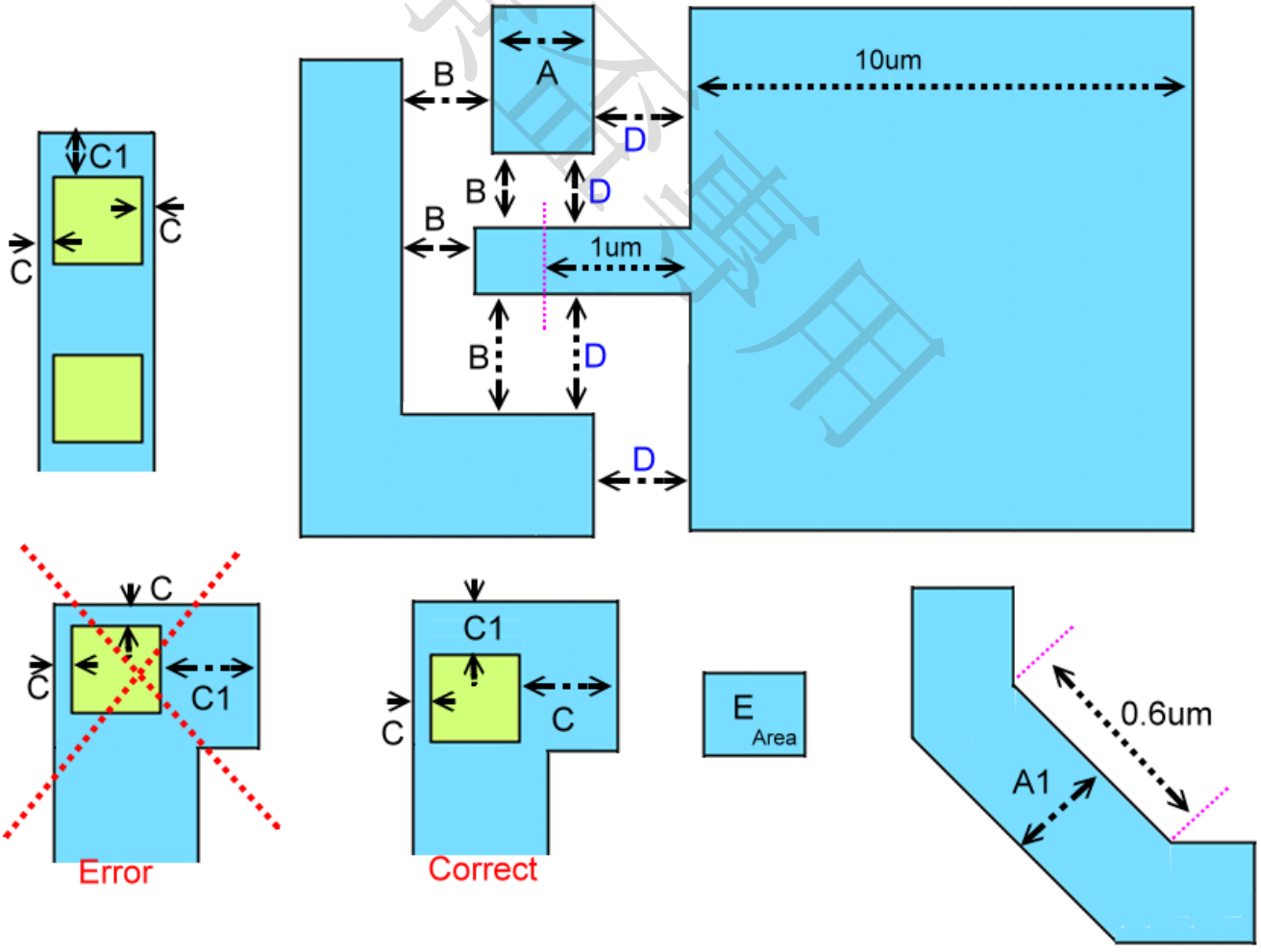
## Contact Rule

| Rule No. | Description Layout | Rule |
|---|---|---|
| Layer : CO | Contact Window | |
| CO.W.1 | Minimum and maximum width of a CO region | A = 0.15 um |
| CO.S.1 | Minimum space between two CO regions | B >= 0.15 um |
| CO.C.1 | Space to 1.0V Gate<br>Space to 2.5V Gate | C >= 0.1 um<br>C >= 0.12 um |
| CO.C.2 | Minimum clearance from a CO on PO region to an OD region | D >= 0.14 um |
| CO.E.1 | Minimum extension of an OD region beyond a OD CO region. | E >= 0.08 um |
| CO.E.2 | Minimum extension of a PO region beyond a Poly CO region. | F >= 0.08 um |
| CO.R.1 | CO on gate region is forbidden | |
| CO.R.2 | Butted Contact is not allowed. | |



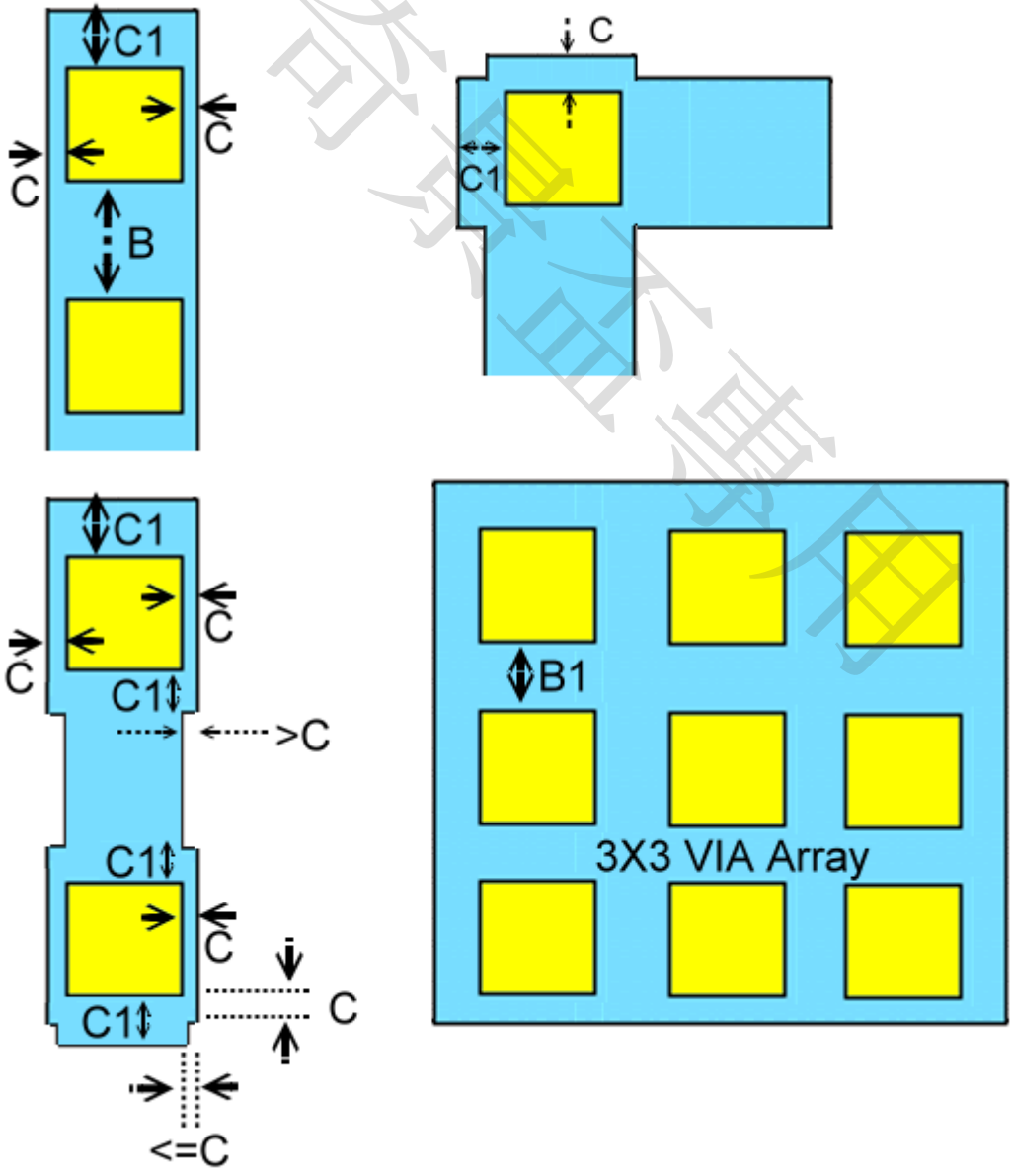
## Metal-1 Rule

| Rule No. | Description Layout | Rule |
|---|---|---|
| Layer : Metal 1 | Metal 1 | |
| M1.W.1 | Minimum width of a M1 region | A >= 0.15 um |
| M1.W.2 | Width of 45-degree bent M1 (length >=0.6 um) | A1 >= 0.18 um |
| M1.S.1 | Space | B >= 0.16 um |
| M1.S.2 | Space to wide M1(both metal line width and length >10um) | D >= 0.8 um |
| M1.EN.1 | Enclosure CO | C >= 0.01 um |
| M1.EN.2 | Enclosure of CO (at least two opposite sides)<br>For CO located at the 90-degree corner, at least one side of the metal enclosure must be treated as the end-of-line and another side can follow the M1.EN.1 rules | C1 >= 0.06 um |
| M1.A.1 | Metal 1 area | E >= 0.124 $um^2$ |



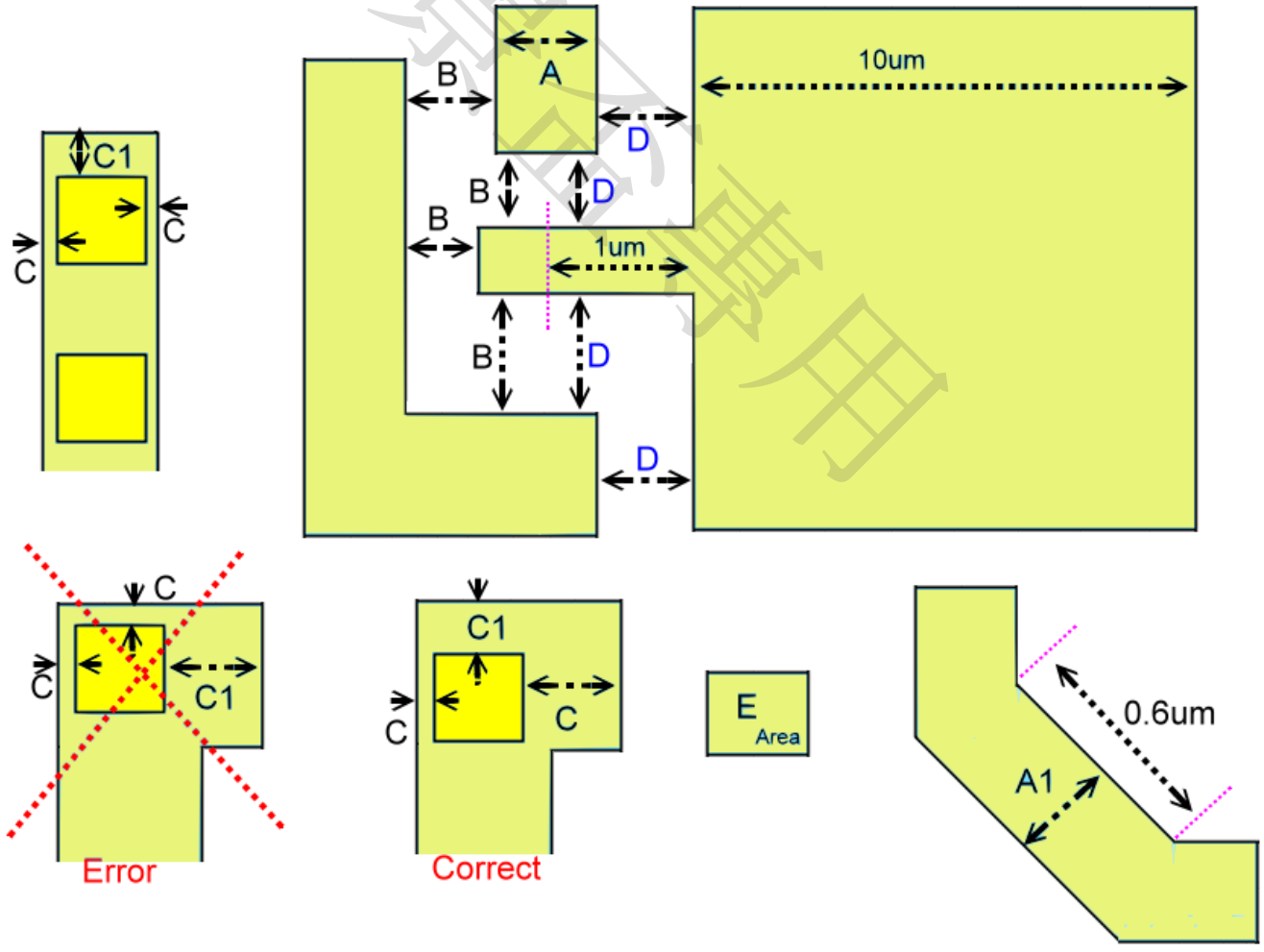
## Via1 Rule

| Rule No. | Description Layout | Rule |
|---|---|---|
| Layer : VIA1 | Via1 Hole | |
| VIA1.W.1 | Minimum and maximum width of a VIA1 region | A = 0.2 um |
| VIA1.S.1 | Minimum space between two VIA1 regions | B >=0.2 um |
| VIA1.S.2 | Space in VIA1 array (VIA1 number >=3X3(row and column>=3) with space <=0.3um | B1 >= 0.3 um |
| VIA1.E.1 | Enclosure by M1 | C 0.01 um |
| VIA1.E.2 | Enclosure by M1(at least two opposite sides) | C1 0.04 um |



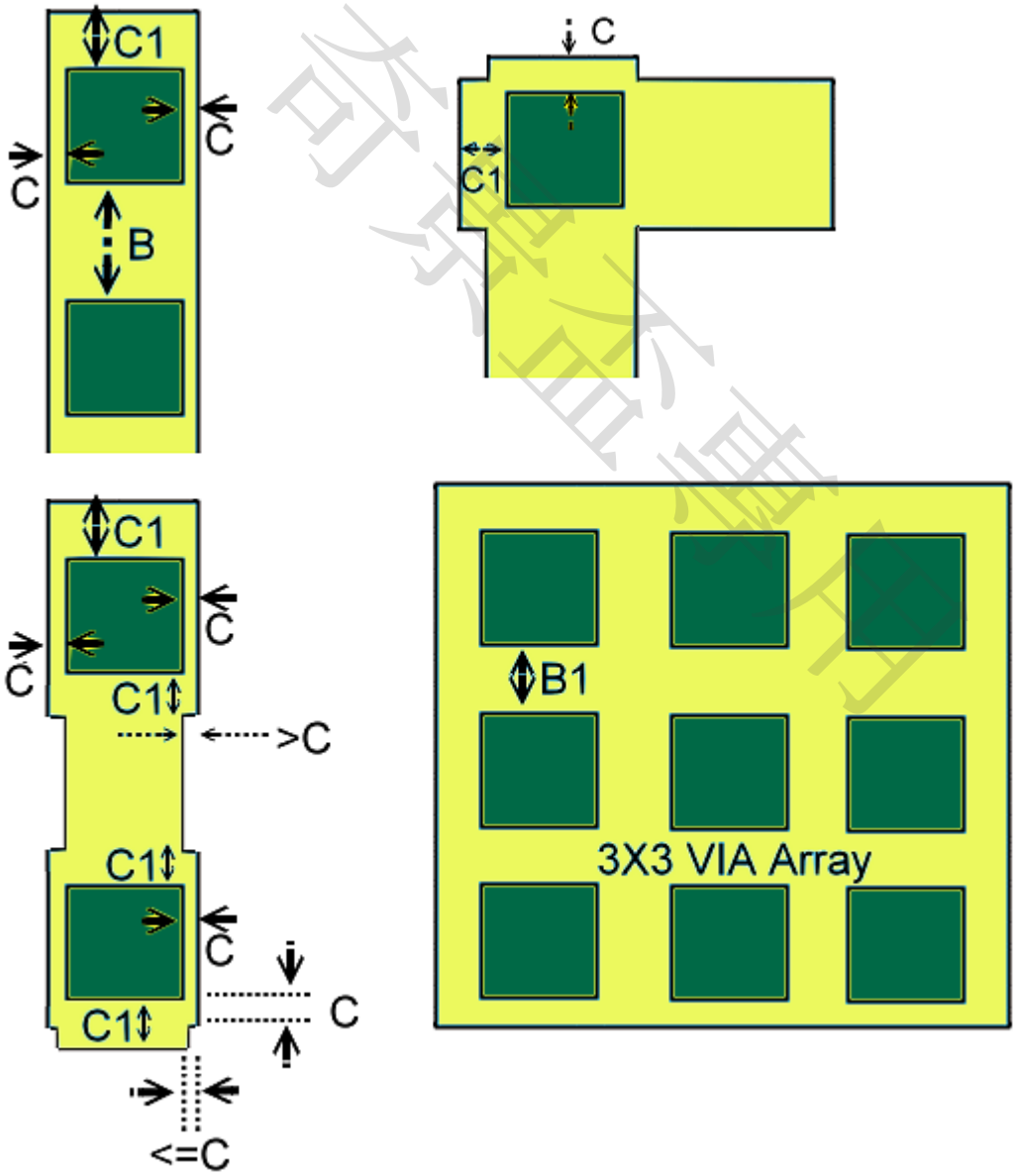
## Metal-2~3 Rule

| Rule No. | Description Layout | Rule |
|---|---|---|
| Layer : Metal 2/3 | Metal 2/3 | |
| Mx.W.1 | Minimum width of a Mx region | A >= 0.22 um |
| Mx.W.2 | Width of 45-degree bent Mx (length >=0.6 um) | A1 >= 0.26 um |
| Mx.S.1 | Space | B >= 0.2 um |
| Mx.S.2 | Space to wide Mx(both metal line width and length >10um) | D >= 0.8 um |
| Mx.EN.1 | Enclosure VIA | C >= 0.01 um |
| Mx.EN.2 | Enclosure of VIA (at least two opposite sides)<br>For VIA located at the 90-degree corner, at least one side of the metal enclosure must be treated as the end-of-line and another side can follow the Mx.EN.1 rules | C1 >= 0.06 um |
| Mx.A.1 | Metal 2/3 area | E >= 0.146 $um^2$ |



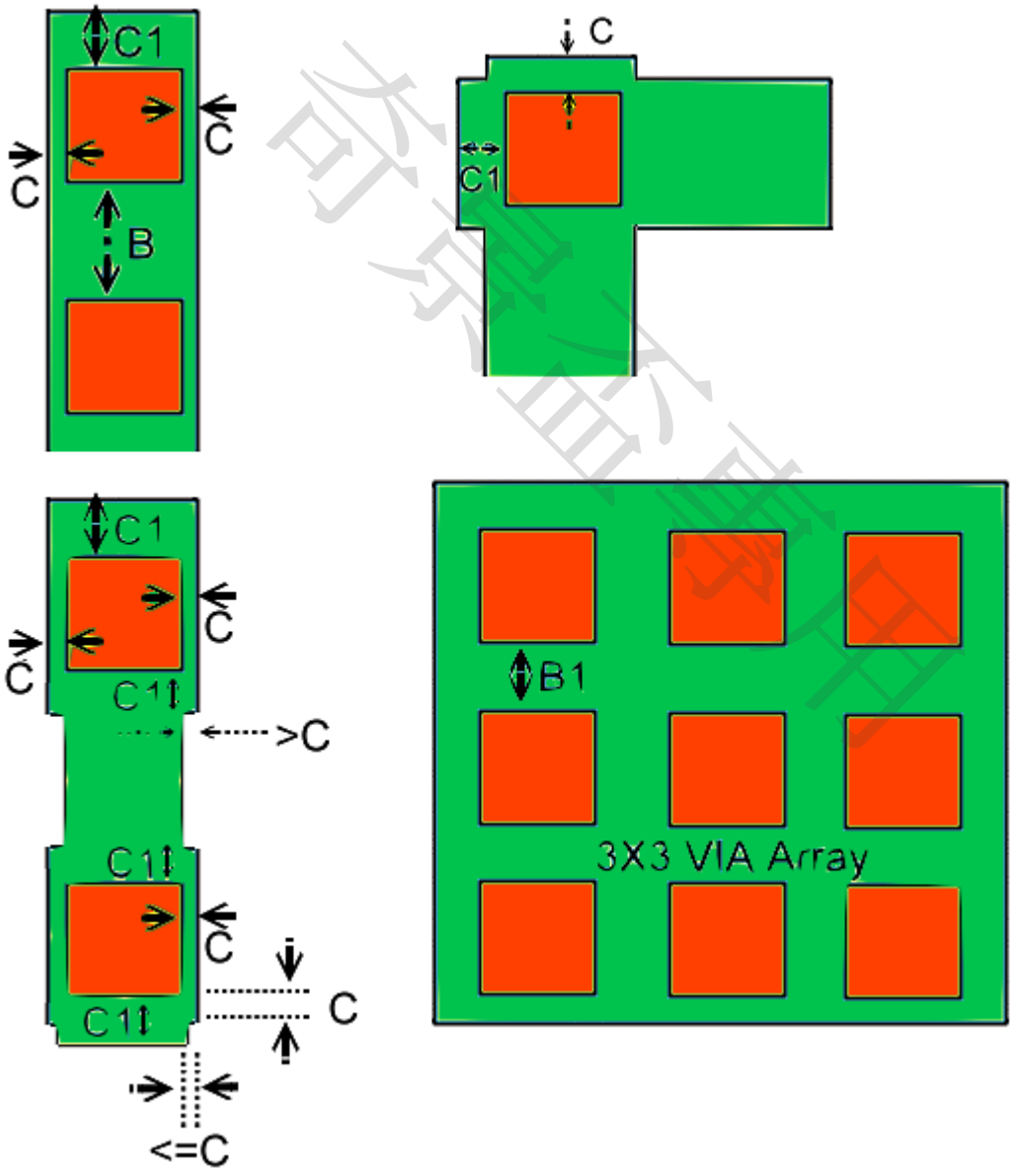
## Via2 Rule

| Rule No. | Description Layout | Rule |
|---|---|---|
| Layer : VIA2 | Via2 Hole | |
| VIA2.W.1 | Minimum and maximum width of a VIA2 region | A = 0.2 um |
| VIA2.S.1 | Minimum space between two VIA2 regions | B >=0.2 um |
| VIA2.S.2 | Space in VIA2 array (VIA2 number >=3X3(row and column>=3) with space <=0.3um | B1 >= 0.3 um |
| VIA2.E.1 | Enclosure by M2 | C 0.01 um |
| VIA2.E.2 | Enclosure by M2 (at least two opposite sides) | C1 0.04 um |



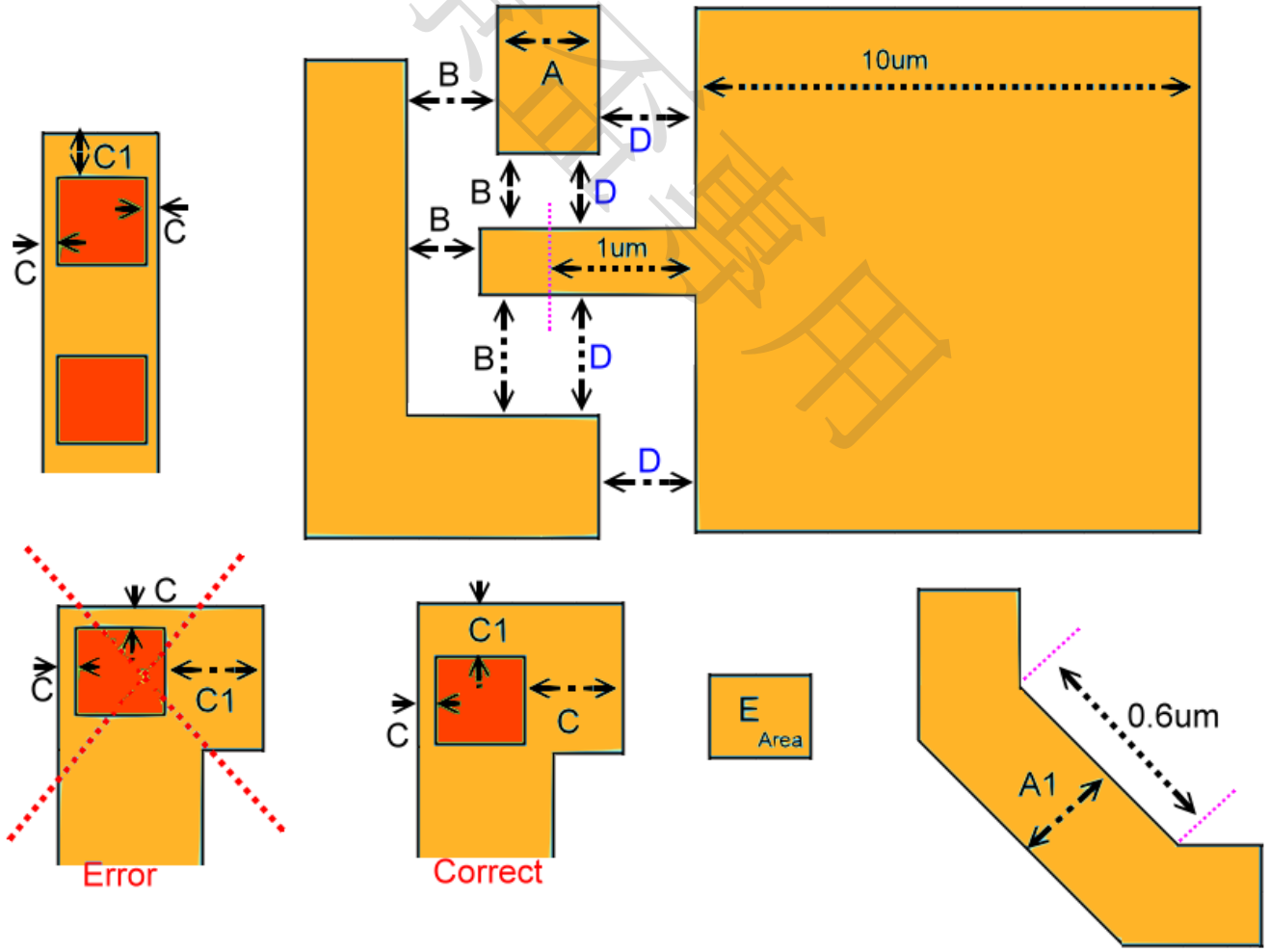
## Via3 Rule

| Rule No. | Description Layout | Rule |
|---|---|---|
| Layer : VIA3 | VIA3 Hole | |
| VIA3.W.1 | Minimum and maximum width of a VIA3 region | A = 0.3 um |
| VIA3.S.1 | Minimum space between two VIA3 regions | B >=0.3 um |
| VIA3.S.2 | Space in VIA3 array (VIA3 number >=3X3(row and column>=3) with space <=0.3um | B1 >= 0.4 um |
| VIA3.E.1 | Enclosure by M3 | C 0.01 um |
| VIA3.E.2 | Enclosure by M3(at least two opposite sides) | C1 0.04 um |



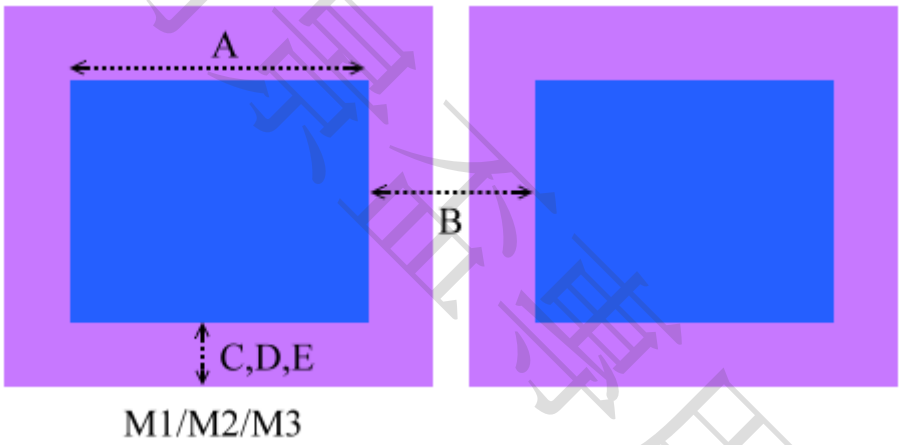
## Metal-4 Rule

| Rule No. | Description Layout | Rule |
|---|---|---|
| Layer : Metal 4 | Metal 4 | |
| M4.W.1 | Minimum width of a M4 region | A >= 0.45 um |
| M4.W.2 | Width of 45-degree bent M4 (length >=0.6 um) | A1 >= 0.45 um |
| M4.S.1 | Space | B >= 0.45 um |
| M4.S.2 | Space to wide M4(both metal line width and length >10um) | D >= 0.8 um |
| M4.EN.1 | Enclosure VIA3 | C >= 0.02 um |
| M4.EN.2 | Enclosure of VIA3 (at least two opposite sides)<br>For VIA3 located at the 90-degree corner, at least one side of the metal enclosure must be treated as the end-of-line and another side can follow the Mx.EN.1 rules | C1 >= 0.1 um |
| M4.A.1 | Metal 4 area | E >= 0.55 $um^2$ |



## Passivation Rule

| Rule No. | Description Layout | Rule |
|---|---|---|
| Layer : CB | Passivation Window | |
| CB.W.1 | Minimum dimension of a CB region for bonding pad | A 80.0 um |
| CB.S.1 | Minimum space between two CB regions for bonding pad. | B 12.0 um |
| CB.E.1 | Minimum and maximum extension of a M1 region over a CB region. | C 6.0 um |
| CB.E.2 | Minimum and maximum extension of a M2 region over a CB region | D 6.0 um |
| CB.E.3 | Minimum and maximum extension of a M3 region over a CB region | E 6.0 um |



## 4. Device & Well Junction Breakdown Voltage

| Description | Breakdown（V） |
|---|---|
| P-WELL <->DNW（LV/MV device） | 12 |
| N+OD<->P-WELL （LV） | 4.5 |
| N+OD<->P-WELL （MV） | 6.5 |
| P+OD<->N-WELL （LV） | 4.5 |
| P+OD<->N-WELL （MV） | 6.5 |
| N-WELL<->P-WELL （LV） | 7.5 |
| N-WELL<->P-WELL （MV） | 8.5 |